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10/786,716	02/23/2004	Douglas A. Larson	188909/US/2	2759

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EXAMINER	
DAVENPORT, MON CHERI S	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,716	LARSON, DOUGLAS A.	
	Examiner	Art Unit	
	Mon Cheri S. Davenport	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-40* is/are rejected.

7)☒ Claim(s) *41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/17/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

1. **Claims 37 and 38** objected to because of the following informalities: Regarding Claim 37 "device" should be written as "electronic device". Regarding claim 38 "apparatus" should be written as "electronic device". Appropriate correction is required.

2. **Claim 41** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. **Claims 22-40** rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (applied below) of U.S. Patent No. 6,697,387. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Regarding **Claim 22**, claim 1 of 6,697,387 discloses an electronic device comprising:

a semiconductor chip;

an I/O pin on the semiconductor chip, for transmitting signals to a signal line outside of the semiconductor chip (see claim 1, lines 6-8) ;

a transmitting circuit that is configured to selectively multiplex the plurality of signal lines onto the I/O pin (see claim 1, lines 9-10) ;

an initialization circuit, coupled to the transmitting circuit that selectively configures the transmitting circuit to multiplex at least one of the plurality of signal lines according to selection information and to transmit the selection information through the I/O pin, which is also used for subsequent data transmission(see claim 1, 19-24).

In addition claim 1 of 6,697,387 is more specific than claim 22 of the present application. Conflicting claims in the instant application are not patentably distinct because conflicting claims are broader and generic with respect to the applied reference claims, i.e., an obvious variation. Many decisions support the fact that a broad or generic claim is obvious from a specific claim, i.e., an obvious variation. See In re Van Ornum and Stang, 214 USPQ 761 (CCPA 1982); In re Goodman (CA FC) 29 USPQ2d 2010 (12/3/1993); In re Vogel and Vogel, 164 USPQ 619 (CCPA 1970); In re Berg (CA FC) 46 USPQ2d 1226 (3/30/1998); Eli Lilly and Co. v. Barr Laboratories Inc., 58 USPQ2d 1865 (CA FC 2001). It is well settled that omission of an element and its function in a combination is an obvious expedient if the remaining elements perform the same functions as before. This notion is supported by In re KARLSON, 136 USPQ 184 (1963); In re Nelson, 95 USPQ 82 (CCPA 1952); and In re Eliot, 25 USPQ 111 (CCPA 1935).

Regarding **claims 23-24**, claim 1 of 6,697,387 discloses everything claimed as applied above. In addition, claim 1 of 6,697,387 discloses every single feature further claimed (see claim 1, lines 11-15, and claim 1, lines 16-18).

Regarding **claims 25**, discloses everything claimed as applied above.

further comprising a synchronizing circuit, coupled to the transmitting circuit, the synchronizing circuit sending a reset signal to the transmitting circuit, the transmitting circuit operable to transmit the selection information from the I/O pin upon receiving the reset signal and to subsequently send output signals from the I/O pin, the output signals multiplexed according to the selection information (see claim 2, lines 1-6).

Regarding **claims 26**, discloses everything claimed as applied above.

wherein the receiving circuit is coupled to the synchronizing circuit and operable to receive the reset signal, the receiving circuit receiving the selection information following receiving the reset signal and subsequently de-multiplexing the multiplexed signals according to the selection information(see claim 1, lines 11-15, and see claim 2, lines 1-6).

Regarding **claims 27** discloses everything claimed as applied above.

wherein the initialization information is a signal line identifier(see claim 6, lines 1-4).

Regarding **claims 28**, discloses everything claimed as applied above.

wherein the transmitting circuit is located on the semiconductor chip and the receiving circuit is located off of the semiconductor chip(see claim 3, lines 1-3).

Regarding **claims 29**, discloses everything claimed as applied above.

wherein the receiving circuit is located on the semiconductor chip and the transmitting circuit is located off of the semiconductor chip(see claim 4, lines 1-3).

Regarding **claims 30**, discloses everything claimed as applied above.

wherein the semiconductor chip is a core logic chip that couples together a processor, a memory, and a peripheral bus in a computer system(see claim 4, lines 1-3, and claim 5, lines 1-3).

Regarding **claims 31**, discloses everything claimed as applied above.

wherein the initialization circuit is located externally to the semiconductor chip(see col. 6 , lines 58-59).

Regarding **claims 32**, discloses everything claimed as applied above.

wherein the initialization circuit is configured to initialize the transmitting circuit during a computer system boot up operation(see claim 10, lines 1-4).

Regarding **claims 33**, discloses everything claimed as applied above.

wherein the transmitting circuit includes: a multiplexer for multiplexing the plurality of signal lines onto the I/O pin; and a control circuit that controls the multiplexer so that the at least one of the plurality of signal lines is multiplexed onto the I/O pin(see claim 12).

Regarding **Claim 34**, claim 13 of 6,697,387 discloses an electronic device comprising: an I/O pin; a semiconductor chip coupled to the I/O pin and comprising a receiving circuit that is configured to selectively de-multiplex signals from the I/O pin onto a plurality of internal signal lines, the receiving circuit having a reset line and being configured to receive configuration data

through the I/O pin upon receiving a signal on the reset line and to thereafter de-multiplex signals from the I/O pin according to the configuration data(see claim 13, lines 14-38).

Regarding **claim 35**, discloses everything claimed as applied above.

wherein the semiconductor chip is a first semiconductor chip, the device further comprising a second semiconductor chip coupled to the I/O pin and the reset line and including a transmitter, the transmitter operable to transmit configuration data from the I/O pin upon receiving a signal on the reset line and to subsequently send multiplexed signals from the I/O pin according to the configuration data(see claim 18, lines 1-2, (see claim 13)) .

Regarding **claim 36**, discloses everything claimed as applied above.

wherein the configuration data is one or more signal line identifiers each corresponding to one of the plurality of signal lines(see claim 13, lines 21-27).

Regarding **claim 37**, discloses everything claimed as applied above.

wherein the transmitting circuit and the receiving circuit are driven by a common clock signal coupled to both the transmitting circuit and the receiving circuit(see col. 7, lines 34-36).

Regarding **claim 38**, discloses everything claimed as applied above.

wherein the reset signal is sent to the transmitting circuit and the receiving circuit during a computer system boot up operation(see claim 13, lines 21-34).

Regarding **claim 39**, claim 13 of 6,697,387 discloses a method for multiplexing signals comprising: exerting a reset signal on a semiconductor chip having a transmitter circuit and an initialization circuit, the initialization circuit receiving the reset signal and causing the transmitter to serially transmit configuration information on a single I/O pin; transmitting data signals to the transmitter over a plurality of signal lines coupled to the transmitter; and the transmitter multiplexing the data signals from selected lines of the plurality of signal lines on the I/O pin, the selected lines being identified by the configuration information(see claim 19, lines 10-28, and claim 20, lines 1-4).

Regarding **claim 40**, discloses everything claimed as applied above.

wherein the semiconductor chip is a first semiconductor chip, the method further comprising receiving the configuration data at a second semiconductor chip including a receiving circuit, the receiving circuit de-multiplexing the data signals according to the configuration data(see claim 18, lines 1-2,(see claim 13).

3. **Claims 39-40** rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims (applied below) of U.S. Patent No. 6,678,287. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Regarding **claim 39**, claim 1 of 6,678,287 discloses a method for multiplexing signals comprising: exerting a reset signal on a semiconductor chip having a transmitter circuit and an initialization circuit, the initialization circuit receiving the reset signal and causing the transmitter to serially transmit configuration information on a single I/O pin; transmitting data signals to the transmitter over a plurality of signal lines coupled to the transmitter; and the transmitter multiplexing the data signals from selected lines of the plurality of signal lines on the I/O pin, the selected lines being identified by the configuration information(see claim 1, lines 1-24).

Regarding **claim 40**, discloses everything claimed as applied above.

wherein the semiconductor chip is a first semiconductor chip, the method further comprising receiving the configuration data at a second semiconductor chip including a receiving circuit, the receiving circuit de-multiplexing the data signals according to the configuration data(see claim 18, lines 1-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mon Cheri S. Davenport whose telephone number is 571-270-1803. The examiner can normally be reached on Monday - Friday 8:00 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MD/md
July 20, 2007

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